Product Design Enhancement with Test Structures for Non-Contact Detection of Yield Detractors

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***Abstract*— Detection and monitoring of the yield loss mechanisms and defects in product chips have been a subject of extensive efforts, resulting in multiple useful Design-for-Manufacturing (DFM) and Design-for-Test (DFT) techniques. Defect inspection techniques extend optical inspection further into sub-10 nm nodes, but many buried defects are formed as a result of multi-layer 3-D interaction, and they are difficult to detect by surface optical scans. In case of a functional failure related to a defect (an open or a short), the localization of the fail site for failure analysis and root cause identification is often difficult, especially for random logic design. In this paper we describe a new -DFM methodology which inserts into the product design special test structures to support New Product Introduction (NPI) and a product yield ramp. The structures are part of PDF Solutions' proprietary Design-for-Inspection (DFI) system with no penalty to the product layout. They are designed to be electrically tested in a non-contact way using a dedicated and specially optimized e-Beam tool. The layouts of these structures are based on the standard cell design therefore they can be used as filler cells in standard cell-based logic designs. The paper presents the concept of the test structures and their design to cover specific failure modes and enable fail mechanism identification. We describe the design flow to integrate the structures into the product floorplan and the non-contact test methodology to scan product wafers and detect failures. Finally, we demonstrate usage of such DFI structures and provide results collected from scanning product wafers containing embedded DFI filler cells.**

***Index Terms* — Design for Manufacturing, Test Structure, E-beam, Defect, Inspection, Characterization, Standard Cells, Yield**

I. INTRODUCTION

SILICON IC manufacturing at the advanced nodes is becoming more and more challenging. The complexity of the technology with increasing number of new processing steps puts a pressure on technology development to deliver the technology with a growing risk that many failure modes may not be fully characterized and quantified before qualification. Consequently, defect reduction, process control, and yield improvement play an even more important role and responsibility of fab operations, which also need to support new product introduction (NPI) activity and ramp high volume production. These tasks become more difficult and resource consuming, due to shrinking dimensions of design features and complex process architectures. As device critical dimensions continue to shrink, new device architectures emerge to meet device scaling challenges. The current workhorse of the device space is the FinFET transistor with a complicated 3D structure. Many device issues, yield and reliability killer defects are the result of interactions between lithography, etch, and fill. In-line metrology and top-down defect inspection is not capable of finding and capturing all issues, many of which have a very local character, or appear as buried defects after a sequence of processing steps. Increasing number of self-aligned steps depends on etch selectivity to provide wider process window for alignment and patterning, but process variability often drives unexpected defects in the form of leakages, or soft opens. Fig. 1 illustrates an example of a failure mode related to contact-to-gate short. Its risk increased substantially with reduced gate pitch and the move from the planar MOSFET to FinFET technology (a new integration scheme was developed in [2] to mitigate this risk). Such failure modes are rarely detected during wafer processing, and often not captured until electrical test of scribes (if there is an adequate test structure coverage) or during the final product test of SRAM and logic blocks.

Among existing in-line detection solutions, the e-beam based Voltage Contrast (VC) technique is the closest one to electric test with a capability to detect buried defects. It has been proven as an extremely valuable technique for detection of electrical shorts and opens in situations where optical inspection tools are ineffective. In the development line, VC inspection is used for SRAM sampling, or testing of dedicated large area defectivity structures, however, the inspection speed is rather slow. Also, because of the low throughput and raster

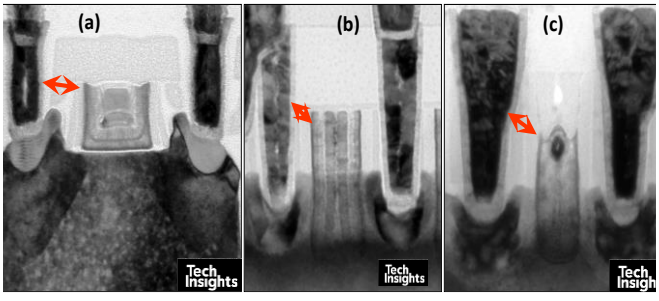

Fig. 1. Illustration of a reduced contact-gate distance (arrows) and higher shorting risk with transition from planar 20nm MOSFET transistor (a) to FinFET transistors in 14/16 nm node (b-c) [1]. To reduce the risk of shorts in the case of (b) and increase process margins, a self-aligned contact process (c) was proposed in [2]. (Images reproduced with permission from TechInsights)

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scan mode, the scanned areas rarely represent all possible layout configurations sensitive to process marginalities.

PDF Solutions' DFI™ system application for DFM, which we described in this work, was first presented by us at Microelectronics Test Structure Conference [3]. This paper expands and explains in more detail this new concept of defect detection. It provides a unique capability of collecting yield and reliability-relevant information by non-contact testing of miniature test structures embedded in product design.

VC-based test structures have been used for quite some time [4, 5], but only on test chips or as dedicated test structures outside of the product die area. Our contribution in this area using dedicated vector eBeam tool was presented in our earlier publications [6, 7]. Product-related DFM solution described in the following sections provides monitoring capabilities for the failure modes representative of the design style and the logic blocks inside the product chips on production wafers. The modifications to the product layout can be considered a DFM (Design for Manufacturing) technique, since it can be used to identify yield detractors and help to improve yields of product wafers.

II. DFI Test Structures

A. Target failure modes

There are many failure modes causing open and short failures which can happen in FEOL, MOL, and BEOL (Front-End-of-Line, Middle-of-Line, and Back-End-of-Line). During technology development and for characterization purposes, a large set of test structures, logic circuits, and SRAM blocks are designed on a test chip. Test structures characterize systematic failure modes, process margins, and device parametrics, but they also monitor process defectivity (large area structures) for FEOL, MOL, and BEOL defects causing shorts, opens, or leakages. However, there is no room for such structures on production wafers, where the expensive "real estate" is dedicated to production ICs, and scarce scribe-line area can host only a handful of parametric structures. Yield detractors and defects are found either through in line inspection as visible defects or in the final test of the product, many weeks or even months after the defect was born and existed undetected in the manufacturing process. Some of them could be detected by the VC e-beam inspection mode, but one would have to know the exact locations on the chip to inspect the layout configuration prone to such failure mode.

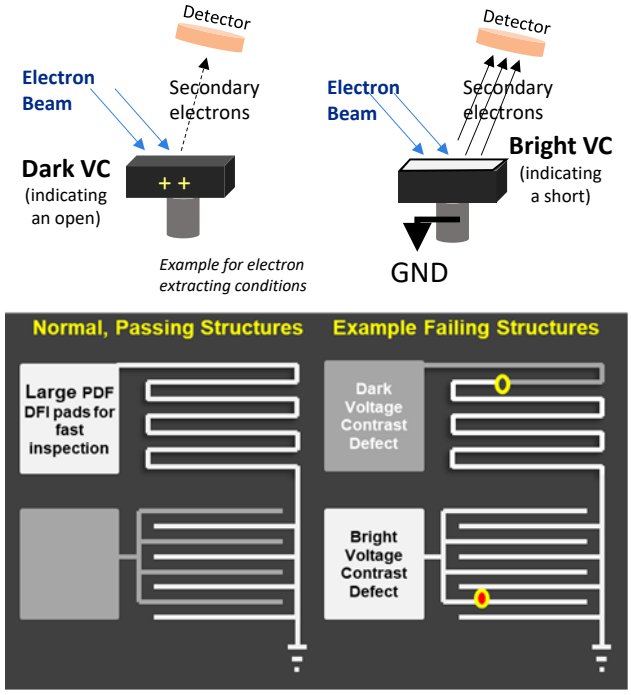

Fig.2. Principle of the e-beam-induced Voltage Contrast used for non-contact detection of Opens and Shorts (Top); and principle of failure detection in a DFI test structure using Voltage Contrast approach (Bottom)

The list of the failure modes – and possible interactions between involved elements (like gate, gate contact, active contact, local interconnect) may be long, and it can be different for each technology and process architecture. Electrical test structures can be designed to monitor each of them, especially the ones which represent 3D buried defects (invisible on the wafer surface during top-down inspection). However, the testability of those structures is still a problem – large size of the probe pads makes them difficult to use on product wafers outside of the scribe lines; moreover, in-line probing for early detection of failures requires special pad construction not compatible with the standard product manufacturing flow.

B. Test structure concept and test principle

As stated earlier, it is possible to design an electrically testable test structure for most of the failure modes discussed, but it is difficult to probe them. However, such a test structure could be built to be tested by e-beam, using Voltage Contrast signal as a response signal. The principle for testing Opens and Shorts using Voltage Contrast is shown in Fig. 2. We named the structures designed specifically for VC testing as Design for Inspection (DFI) structures. Each of them has a designated terminal for VC probing, called VC or DFI pad.

DFI pads are built at lowest metal levels to enable early inspection, typically at M0 or M1 layer. The size of the pad can be very small, comparable to the beam size, which can be reduced to tens on nanometers and a similar placement precision. This is a very small test pad size, compared with typical electrical probing pad (which is larger than 25 μm x 25μm). Use of a very small pad for VC inspection has also a benefit of reduced capacitance related to the additional metal pad, which adds to existing capacitance of the structure itself. The VC test time has to take into account the dwell time required to charge the capacitance of the floating features during the test for open or short defects.

Ground connections need to be used to enable Voltage Contrast testability. A failure of the test structure is detected by scanning the DFI test pad of a test structure and comparing its "polarity" (Dark/Bright/Grey) to the library of expected response values [8]. Opens are detected when a DFI filler cell pad for an open failure mode turns dark. When there is no defect, the pad is bright due to the strong secondary electron

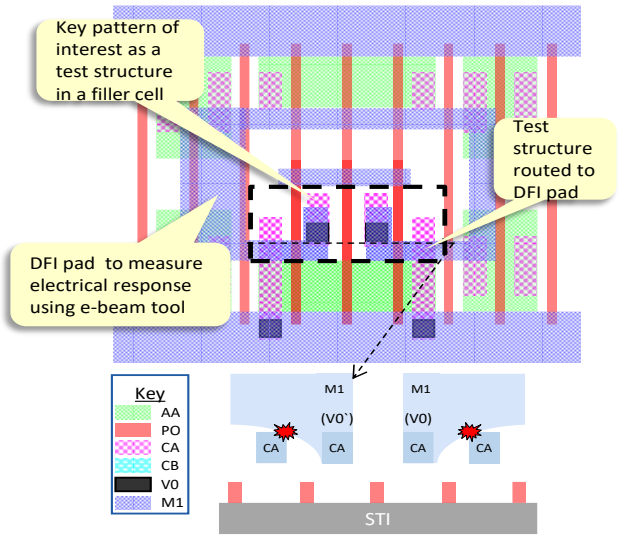

Fig. 3. Example of the DFI Filler Cell with embedded test structure for detection of V0 chamfering short. DFI metal pad is used to "read-out" Voltage Contrast signal from the structure

emission from the grounded pad. Shorts are detected when a DFI filler cell pad turns from normally dark to bright.

A test structure to detect such failure mode can be designed into the shape of a standard cell, as illustrated in Fig. 3. This example shows a structure sensitized to detect lower via (in this case V0) shorts to underlying Local Interconnect due to the so-called chamfering effect (3D bottom trench corner rounding during via/trench etch process). During the test, a via chamfer short will cause a change in the VC response and the DFI pad will be bright instead of expected dark contrast in a healthy structure.

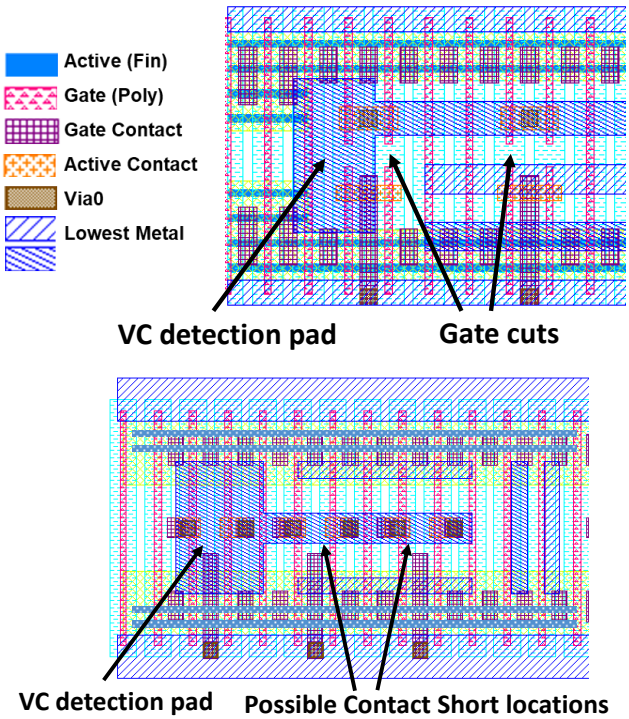

Fig. 4. Examples of implementation of standard cell-like test structures for Voltage Contrast detection of unique failure modes: Gate end-to-end short (top layout) and Gate Contact to Active Contact short (bottom layout) [9]

Other examples are shown in Fig. 4, which shows standard cell-like layouts of test structures sensitized towards gate tip-to-tip shorts and contact shorts [9]. Interestingly, while the gate contact to active contact short can be detected by in-line e-beam scan of a failing product, the gate tip-to-tip short cannot be captured without special pattern modifications (like those performed for our DFI structures).

One of the key elements of the DFI test structure is the selection and construction of the VC test pad, which will be used to determine if the structure is passing or failing. Example of the response of DFI tests structures is shown in Fig.5, where replicates of identical structures were placed within a block of a test chip. The DFI e-beam test system can detect the "dark" or "bright" response, but it also can measure "gray scale" levels corresponding to soft shorts or leakage currents, which extends characterization capabilities beyond simple "hard" shorts and "hard" opens. As a result, the DFI filler cells can detect leakages that represent soft defects which often lead to reliability weaknesses.

We developed a family of test structures to detect all possible failure modes and designed them in a way to sensitize each structure type to a single failure mode [9]. This helps to isolate the failure mechanism and enables easy localization for FA (failure analysis). The focus was specifically to provide the coverage of buried defects and failure mechanisms which could not be observed with top-down optical defect inspection. The exemplary list of such defects is listed in Table 1.

Table 1. Failure mode coverage of the DFI test structures highlighting superior defect detection capabilities compared to typical top-down optical defect inspection

Fail Mode	Mechanism	Inspection detectable	DFI detectable
S/D short to Gate	Trench Cnt to Gate short	No	Yes
	Active Cnt to Gate short	No	Yes
	Gate Cnt to Trench Cnt short	No	Yes
	Active Cnt to Gate Cnt short (top)	Yes	Yes
	Via0 Taper/Chamfer short to Cnt	No	Yes
	M0 Short due to etch or CMP	Yes	Yes
Contact Open	Patterning issue	Yes	Yes
	Fill problem/Void	No	Yes
	Interface problem	No	Yes
Via Open	Patterning issue	Yes	Yes
	Under-Etch, interface problem	No	Yes
	Cu Plating, Cu Voiding	No	Yes

III. DFI Test Structure Design

Typical product chip logic blocks, designed using a standard cell library, have about 80-90% area utilization, limited by

routing congestion. The remaining 10-20% end up being filled by the so-called filler cells [10]. For the chips designed in most advanced nodes of 5 nm and below it could represent tens to hundreds of millions of cells. DFI filler cells, proposed in this work, are designed to be very similar to the filler cells for a given standard cell library, but they are modified to be sensitive to a particular failure mode of interest and include a VC pad for high throughput non-contact test. Such cells can then be used instead of the originally designed dummy fill cells, which have no functional purpose (sometimes they are designed and used as decoupling capacitors). This concept is illustrated in Fig. 5, where the original filler cells are replaced by DFI instrumented filler cells.

A. Standard Cell – based test structures

DFI filler cells are designed and customized for a specific standard cell library. The DFI filler cells design must follow the same design rules, and they must be DRC (Design Rule Check) clean after insertion into the product. Therefore, the cells must adhere to all cell boundary designs of the standard cell library such as power rail width and left/right boundary position.

All test structures embedded within the DFI filler cell are 2-terminal elements. One terminal serves as the DFI pad which will be scanned by the e-beam. The second terminal is a "ground" terminal which serves as the source of secondary electrons during the e-beam scan. The best ground source is a node electrically connected to the Pwell/Psub. An alternative ground is the source/drain of a PFET (P+ in Nwell diode).

The DFI filler design must be optimized around several competing factors. The test structure layout design must be able to stimulate the target failure mode with minimal sensitivity to secondary failure modes. The size of the DFI filler cell should be minimized in order to maximize the insertion rate. To maximize the e-beam response on the DFI pad, the best grounding source should be used, and any other possible secondary leakage paths should be eliminated or minimized. Most importantly, the test structure should be designed so that it does not increase the product sensitivity to process defects, i.e., it should not impact product yields or performance.

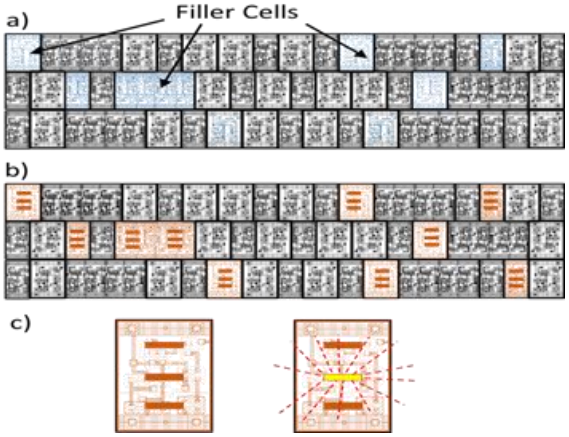

Fig. 5. Illustration of the concept of replacing Logic filler cells in a block of CMOS standard cells with DFI cells of the same size: (a) original Std cell block with fill cells; (b) replacement of the filler cells with DFI filler cells; (c) VC response of DFI filler cell during a test with e-beam tool

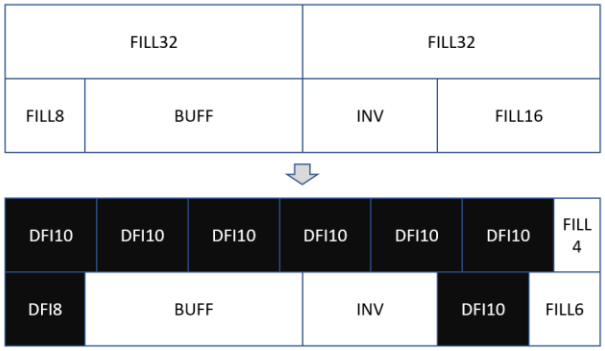

Fig. 6. Example showing that one or more filler cells can be replaced with one or more DFI cells.

To complete a DFI filler cell library, all variants of gate length and threshold voltage (VT) options must be generated. During the insertion flow, the appropriate gate length and VT variant will be selected for insertion to match the attributes of the target logic block. A typical DFI filler cell library may consist of hundreds to thousands of cells.

B. Insertion in the Product Design

DFI filler cells are swapped into individual design blocks or the design top level immediately after filler cells are inserted. The number and size of the DFI filler cells inserted does not need to match the number or size of the removed filler cells as shown in Fig. 6. Any filler space not fillable by DFI filler cells is reverted back to filler cells but not necessarily by cells of the same size. The DFI cell insertion tool ensures that cells added to the design always match the threshold voltage and the gate length of the original filler cells that are being replaced. This keeps the design DRC clean and prevents device performance changes for neighboring active logic cells.

In a place and route tool agnostic flow, filler cells are exported into a DEF (Data Exchange Format) file and deleted from the layout database. The DEF file is used by the DFI cell insertion tool to generate an incremental DEF file containing DFI filler cells. The incremental DEF is then read into the place and route database. The full Place and Route (P&R) design flow including DFI cell swap is shown in Figure 7.

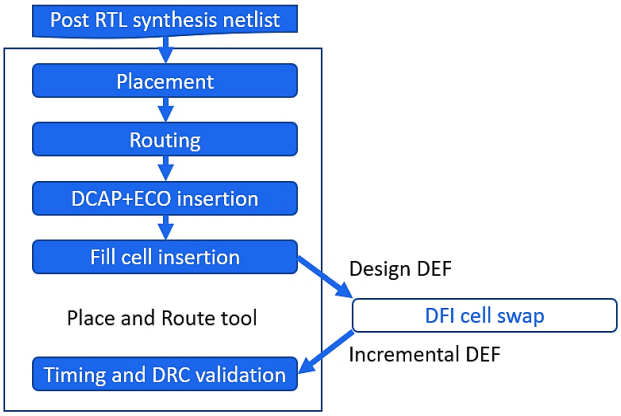

Fig.7. Place and Route design flow including DFI cell insertion

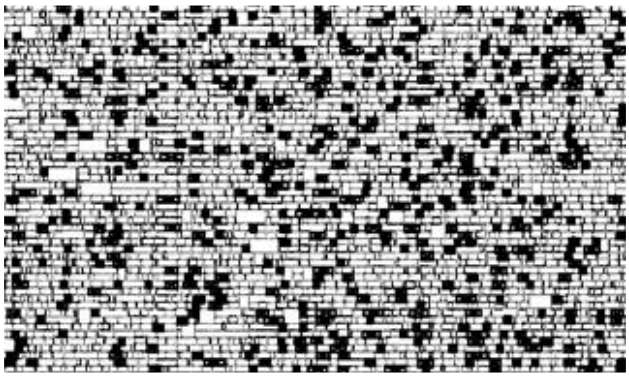

Fig. 8. Clipped layout image of a standard cell block showing a typical DFI cell distribution. White boxes are original standard cells from the original block design. Black boxes are DFI filler cells (containing DFI pad for e-beam testing)

Multiple experiments are placed in a single DFI filler cell library. The DFI cell insertion tool has a control parameter to adjust the weighting of experiments to achieve the desired balance between different failure modes and required detection sensitivity (observability levels).

Figure 8 shows a typical distribution of DFI cells in a standard cell logic block. Note the regions of high and low DFI cell density. Typical DFI cell density across an entire die is within 1-5% of logic area (not all filler cells are replaced by DFI filler cells). Because of the sparse distribution of DFI cells, an e-beam testing tool is required that only attempts to rasterize the areas of interest – the DFI cells, and skips over logic cell area

IV. Test of DFI structures and Data Analysis

As indicated earlier, the only feasible way to electrically test such small structures with a high throughput is e-beam based VC. Fig 9. shows an example of a failure detected in one of the filler cells in a demonstration test block built using identical cells dedicated to a single failure mode. The picture illustrates the SEM (Scanning Electron Microscopy) view of the block with a visible failing structure. However, to detect a defect across all the structures one does not need to scan the whole area – it is enough to look at the VC pads only.

Therefore, if we set an objective to scan only the DFI test structures, and only their VC pads, then the challenge for the e-beam testing system is to achieve high efficiency, sensitivity, and throughput by testing VC pads only.

A. DFI inspection system

The DFI system that we built includes DFI filler cells, e-beam test tool, and analysis software. A dedicated PDF Solutions proprietary e-beam tool (eProbe® inspection machine) has been designed and optimized to enable testing of ~ 2-10 billion DFI pads/hour [11]. The tool concept takes advantage of the vector scan vs traditional raster scan which enables significant reduction of the scan time by skipping a "non-productive" area (Fig. 10).

To support the DFI filler cell test, the test program of the eProbe tool is prepared using the placement coordinates of the cells of interest and their expected secondary electron

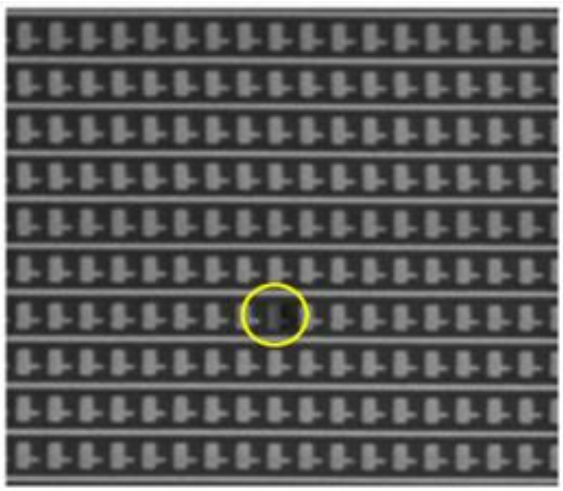

Fig. 9. Example of a failure detected by one of the identical DFI Filler Cells arranged in a single design block. The DFI metal test pads are illuminated by e-beam tool in a raster mode

response when the e-beam is applied to them. Additional components are added to the test program to ensure the e-beam is always "on-track" within the die and the standard cell block and makes alignment corrections as needed.

B. Dark-Bright VC Calibration

As mentioned before, instead of rastering images, the eProbe tools apply the e-beam directly towards the points of interest (VC pads) to collect read-outs of secondary electrons or "grey-levels". If a grey-level deviates from the expected value by a threshold, that specific location is tagged as a potential defect.

The grey levels of potential defects are not simply categorized into binary Opens (Dark VC) or Shorts (Bright VC response) but translated to their likely leakage or resistance values. A model is created for the purpose of translating observed grey level values in relation to reference grey levels to their expected leakages or resistances. However, the coefficients of the model do need to be extracted based on actual leakage vs. grey level correlation.

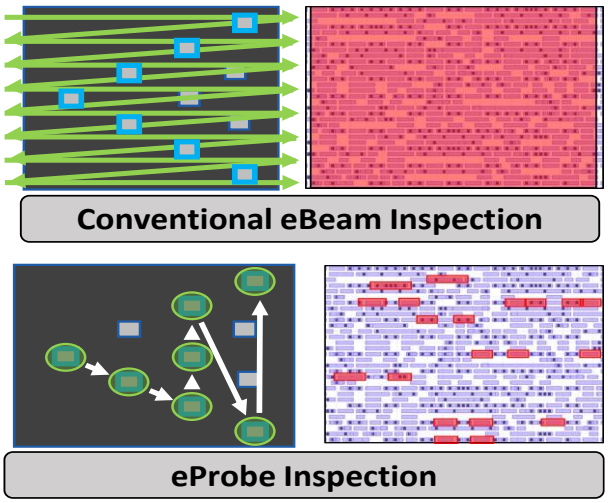

Fig. 10. Acceleration of eBeam inspection of DFI filler cells with a specialized vector scan tool (eProbe®)

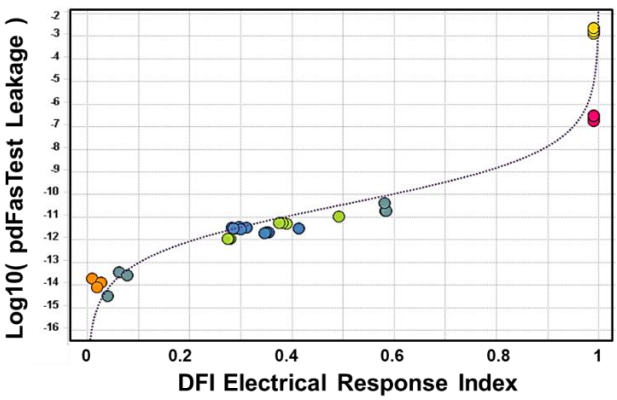

Fig. 11. Calibration of the VC response (Grey Levels) with dedicated test structures designed for electrical testing (part of PDF CV® characterization infrastructure). DFI Electrical Response Index values are normalized using the highest and the lowest values

One approach is to perform nano-probing to find the leakage values on the cells that have been scanned. Another method to determine the coefficients for the model is to include reference e-beam structures with known "designed in" leakage/resistance values to scan, as proposed in [12]. In our experiments we designed DFI structures as part of a block of electrically testable structures [13]. All structures scanned by eProbe tool in such blocks were then processed to higher metal levels and tested by parametric tester (in this case addressable arrays from PDF Solutions' CV® design and pdFasTest® parallel electrical tester was used). The results shown in Fig. 11 demonstrate that it is possible to distinguish between leakages in the pA and nA range, but the VC technique may not be able to distinguish between soft shorts with resistances below 1MΩ (above the μA current range).

V. DFI Applications and Results

As an example of implementation, a set of DFI filler cells were embedded in a product designed and manufactured in advanced FinFET technology. The DFI cells were sensitized to detect critical fail modes with an emphasis upon the FEOL

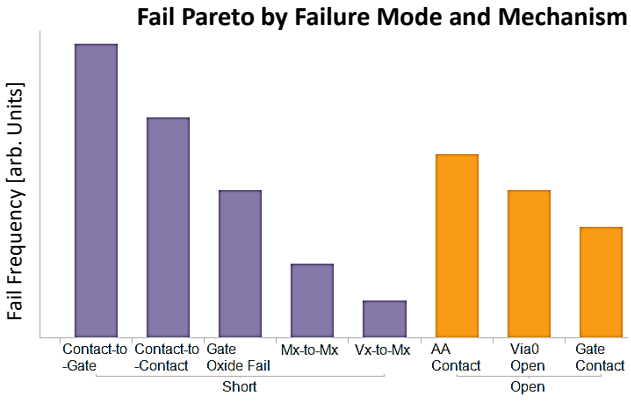

Fig. 12. Results of DFI filler cell measurements. Fail Count pareto summarizes failures from top failure modes among those represented in filler cells. For this case, Shorts dominate the pareto, with Opens showing lower fail rates. The fail counts correspond to ppb range.

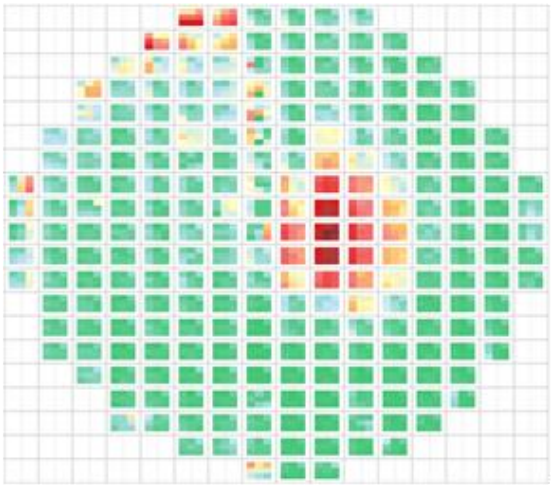

Fig. 13. Wafer map of a failure mode detected by an in-line DFI filler cell scan on an excursion wafer

and MOL. Dozens of fail modes were observable with these DFI filler cells spanning across a DOE of layout configurations. More than 100 million DFI structures were embedded in the product logic area per die, which added up to billions of structures per wafer.

The wafers were scanned with an eProbe tool, inspecting only DFI filler cells (only the DFI pads). The grey level response of each DFI test pad was collected and compared with the modeled, predicted value for healthy structures (stored in the database) to identify failing locations. The failures were later classified by failure mode and die/wafer location.

Fig. 12 shows the results from the DFI filler cell measurements performed on a single wafer. The aggregate fail count per fail mode is shown in the form of a pareto. Fail modes corresponding to shorts are shown in blue while fail modes shown in orange reflect opens. Based on DFI pareto, the dominating failures are from the Contact module, due to shorts between Contact-to-Gate and Contact-to-Contact. For wafers with particularly high failure rates, wafer maps were generated for each of the failure modes (as well as the combined die yield maps). Fig. 13 provides an example of a wafer map for one particular failure mode illustrating the distribution of the fails across the wafer and within each die. Such spatial coverage and resolution is possible because of very high count and spatial density of DFI test structures embedded in the product design.

Another valuable benefit from the DFI filler cells is that they enable targeted FA to determine failure mechanism and possible root cause. In such case, failure mode identification and localization within the die block does not require complicated circuit analysis. The FA can be done on the product wafer immediately after detecting the yield threatening process excursion, or after finishing full processing, if the expected overall yield is good. The fail location is known down to the cell level (from DFI scan and analysis), and FA can be performed on one of the failing dies, after dicing and packaging the yielding dies from the wafer.

The failures captured by DFI are real failures, but they do not impact the yield of the product, as they occur in the non-

active part of the circuitry (filler cells). However, they reflect the overall failure statistics on a product wafer. Using the pareto and the failure rates calculated based on measurements from a few percent of the area covered by the DFI filler cells, we can model the yield impact of such fails across all functional standard cells, and associated yield loss.

The DFI system is capable of measuring "gray scale" levels corresponding to soft shorts or leakage currents, which extends characterization capabilities beyond simple "hard" shorts and "hard" opens. Consequently, we believe that the DFI filler cells can help detecting leakages that represent soft defects (two orders of magnitude increase in leakage, compared to healthy structures) which often lead to reliability weaknesses.

VI. Discussion

Traditionally, the vast majority of test structures are placed on test chips and manufactured on dedicated test wafers. However, it is difficult to find room for such structures on product wafers. This makes debugging of yield and manufacturing issues on product wafers difficult and resource costly. Because of higher volumes of product wafers than test chip wafers, placing even small number of test structure replicates can provide significant insight into process issues and yield detractors. Even more, placing test structures inside a product die can be considered a valuable DFM technique to increase the overall sample size, especially if it does not impact the die area and the die cost. Many DFM and DFT (Design for Test) techniques applied to product chips require an extra area not just for the test structure itself, but often much more so to allow communication and test (e.g. PVT - performance, voltage, temperature sensors).

A. Defect detection and observability requirements

Functional product yield is limited by systematic and random failures. They may have different characteristics, spatial signatures, and product design dependencies, but to achieve a good yield on a product in advanced nodes below 10nm, the failure rates for each of the failure modes need to be in sub-ppb range (ppb – parts per billion).

Table 2 shows an example of theoretical counts of design features in a dense 1 cm^2 logic product die, assuming 1 billion transistors. We can estimate the standard cell count and the number of filler cells. We also can estimate the number of occurrences of some of critical features per die (only 3 examples shown) and build a yield model for them. Based on Poisson yield model [14] we show the required failure rates to achieve limited yields of 95% for each failure mode. Finally, we calculate the observability required to detect a 10% excursion of a single failure mode with a 10% yield impact. With ~ 630 dies per wafer, the impact is very significant even with Failure Rates (FR) well below ppb.

Table 2. Feature counts and FR estimates corresponding to 95% and 90% Limited Yields (LY) of some of critical FEOL failure modes

Feature	Count	Failure Mechanism	FR to get 95% LY	# dies failing	FR need to detect 10% excursion
Transistor	1.0E+09				
Std Cells	1.2E+08				
Dummy cells	1.5E+07				
DFI Filler cell	3.0E+07				
Gate cut	1.6E+08	Tip-Tip short	0.3 ppb	~ 30	0.7 ppb
Active Cnt	6.0E+08	Cnt-Gate short	0.1 ppb	~ 30	0.2 ppb
Gate Cnt	3.5E+08	Cnt open	0.15 ppb	~ 30	0.3 ppb

The table also gives an estimated count of the dummy filler cells we can insert by the proposed DFM approach. This number is ~ 30 million/die and ~ 20 billion/wafer. That means that a product wafer can be instrumented with test structures allowing detection of excursion of 0.05 ppb if all structures would be monitoring the same failure mode. That observability can be lower in case when we decide to cover more failure modes, for example, in the case of 10 different modes the observability would decrease to 0.5ppb if failure mechanisms are covered with equal representation. The observability can be better than estimated for some of short failure modes, since a single small DFI structure can have multiple elements tested for failures, as shown in previous examples (e.g., gate tip-to-tip structure in Fig. 4, which has 4 occurrences sensitive to a short). With a dedicated eProbe tool, capable of scanning 10 billion structures per hour, one can focus on 2-3 failure modes for manufacturing process improvement purposes and scan multiple wafers per lot without violating wafer wait time. Alternatively, yield engineers may decide to sample more wafers with lower coverage (e.g. 10% of structures only) for the same cumulative number of test structures and improved observability based on accumulation of tested wafers.

B. Advantages of DFI methodology

The DFI filler cell solution proposes implementing test structures without an area penalty. To achieve that we replace otherwise unused areas on product chips with test structures targeting failure modes causing opens and shorts in FEOL, MOL, and BEOL integration. The proposed method of using DFI filler cell test structures offers several advantages compared with traditional test structures:

- Test structure footprint – the test structure is of the size of a standard cell (sub-micron) replacing existing filler cells.
- No area overhead – There are neither electrical test pads, nor routing or communication circuitry. It is a truly zero-added area implementation.
- In-product representation – the structures detect the failure modes occurring on exactly the same wafers and in the same die regions as the product IP blocks
- In-line testability – non-contact testing of product wafers with low risk of damage or defect creation
- Fast fail site localization – the failure is bound to a single Filler Cell (sub-micron size) with minimum de-processing to reach the defect layer
- Test speed and observability of failure modes unique to random logic design – which is achieved by scanning large

numbers of product wafers with DFI filler cells and a dedicated e-beam tester

- Yield relevant data for targeted process improvement – easily quantified at the pareto level (and at the EWS yield as well) with continuous monitoring of failure modes on product wafers – especially valuable for NPI.

VII. Conclusion

We have proposed a new DFM methodology to detect and monitor key failure modes impacting product yield on production wafers. It converts filler cells used by P&R EDA flow into test structures that can be tested for failures using a high-throughput dedicated e-beam tool. The DFI filler structures can be embedded in the product design with no area penalty and no performance/yield impact. The system includes a DFI EDA insertion flow that allows product designers to easily insert the DFI cells during the regular product design phase. We implemented a contactless inspection tool which is optimized to quickly jump between the inserted DFI filler cells. The infrastructure allows fast generation of design specific inspection recipes, as well as analysis of the e-beam test data and quantification of the failure rates. Furthermore, the DFI system can provide cloud-based data exchange and data analysis to enable collaboration between the fabless design community and the manufacturer.

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